C2 cont'd. 32. (New) The voltage-driven power semiconductor device according to claim 27, wherein said gate is a trench-type gate embedded in said opposing side.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 23-32 are pending for examination in this application. Claims 23-29 have been amended to better clarify the nature of the current sense terminal and new Claims 31 and 32 have been added, all without the introduction of any new matter.

The outstanding Office Action presents an objection to Figures 1 and 2, a rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa et al (U.S. Patent No. 5,874,750, Yanagisawa), and a rejection of Claims 24-30 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda et al (1998 International Symposium article, Takeda).

Turning to the objection made to Figures 1 and 2, it is believed that this objection has been overcome by the attached letter seeking the Examiner's approval of changes to Figures 1 and 2 to add the label "Background Art" thereto.

Before considering the outstanding prior art rejections applied to Claims 23-30, it is believed that a brief summary of the invention thereof would be helpful. In this regard, the present invention involves a chip-like voltage-driven power semiconductor element and power semiconductor device including this element. The element has a collector formed on one side and a gate and main emitter formed on the other side thereof along with a current sense terminal. Current flow is from the collector to both the main emitter and the current sense terminal.

One aspect of the invention involves the element being an injection enhanced gate transistor (IEGT) while another aspect is concerned with sensing current flow and providing for operating with an electron injection efficiency at the main emitter and the current sense terminal of 0.73 or more. Note the explanation of benefits and properties in the specification at page 60, lines 3-12, page 60, line 26-page 61, line 7, as well as at page 73, lines 21-26, for example.

Turning to the rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa, it is noted that all of Claims 23-32 require a "current sense terminal." A current from the collector is split to flow into this current sense terminal and main emitter so that "the current sense terminal" detects a current that flows into the main emitter so that an overcurrent, when detected, can be prevented. This is an important property and advantage of the present invention.

Yanagisawa, on the other hand, shows a voltage sense emitter in FIG. 3, which senses the voltage at the emitter electrode of an IGBT. See the last five lines of the Abstract, col. 4, lines 54-67 and the last two lines of Claim 1 at col. 8 of Yanagisawa. Clearly, Yamagisawa does not disclose a current sense terminal which senses the current flowing into the emitter electrode and itself, it only teaches and suggests emitter voltage sensing.

Furthermore, the outstanding Action errs in considers the limitation of the electron injection efficiency being 0.73 as being an optimum value of a result effective variable, the discovery of which involves only routine skill. However, the conventional IGBT structure adopted by Yanagisawa would have a problem if the electron injection efficiency is provided as 0.73 or more because the injection efficiency would be too high at the emitter. This would prevent the base voltage from controlling the switching operation between the collector and emitter. In contrast, the present invention of Claim 23 does not suffer from this problem at

such a high efficiency, see FIG. 47 and note the IGBT curve and IEGT curve illustrated therein. Thus, it is clear that the electron injection efficiency at the main emitter being 0.73 or greater cannot be considered as an optimum value at which Yanagisawa's device could operate and such an efficiency cannot be derived from Yanagisawa or considered to be obvious over this reference.

In addition, it is well established that the rule of In re Boesch, cited at the top of page 3 of the outstanding Office Action, is not a rule equating any type of routine experimentation to a conclusion of obviousness.

In this regard, In re Antonie, 195 USPQ 6, 8-9 (CCPA 1977) notes that:

> The PTO and the minority appear to argue that it would always be obvious for one of ordinary skill in the art to try varying every parameter of a system in order to optimize the effectiveness of the system even if there is no evidence in the record that the prior art recognized that particular parameter affected the result. As we have said many times, obvious to try is not the standard of 35 USC § 103. *In re Tomlinson*, 53 CCPA 14231, 363 F.2d 928, 150 USPQ 623 (1966). Disregard for the unobviousness of the results of "obvious to try" experiments disregards the "invention as a whole" concept of § 103, *In re Dien*, 54 CCPA 1027, 371 F.2d 886, 152 USPQ 550 (1967) and *In re Wiggins*, 55 CCPA 1356, 397 F.2d 356, 158 USPQ 199 (1968), and overemphasis on the routine nature of the data gathering required to arrive at appellant's discovery, after its existence became expected, overlooks the last sentence of § 103. *In re Saether*, 492 F.2d 849, 181 USPQ 36 (CCPA 1974). [Footnote omitted.]
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> In *In re Aller*, 42 CCPA 824, 220 F.2d 454, 105 USPQ 233 (1955), the court set out the rule that the discovery of an optimum value of a variable in a known process is normally obvious. We have found exceptions to this rule in cases where the results of optimizing a variable, which was known to be result effective, were unexpectedly good. *In re Waymouth*, 499 F.2d 1273, 182 USPQ 290 (CCPA 1974); *In re Saether, supra*. This case, in which the parameter optimized was not recognized to be a result-effective variable, is another exception. The decision of the board is reversed. [Emphasis added.]

The court in Antonie further noted (at 195 USPQ 8) that the consideration of the invention as a whole requires consideration of claimed values such as the electron injection

efficiency value of 0.73 claimed here and the inherent properties of the invention claimed as follows:

> In determining whether the invention as a whole would have been obvious under 35 U.S.C. § 103, we must first delineate the invention as a whole. In delineating the invention as a whole, we look not only to the subject matter which is literally recited in the claim in question (the ratio value) but also to those properties of the subject matter which are inherent in the subject matter and are disclosed in the specification. *In re Davies*, 475 F.2d 667, 177 USPQ 381 (CCPA 1973). In this case, the invention as a whole is the [claimed] value . . . and its inherent and disclosed property.
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> * * *
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> The controlling question is simply whether the differences (namely the [claimed] value . . . and its property) between the prior art and appellant's invention as a whole are such that appellant's invention as whole would have been obvious.

This is the controlling question here as well. The anser to this controlling question is clearly that Yanagisawa does not teach or reasonably suggest the differences here as to the claimed "current sense terminal" or the claimed "electron injection efficiency at said main emitter and said current sense terminal" that "is 0.73 or more," much less the inherent properties associated therewith. Accordingly, it is believed to be clear that Claim 23 and its delineated invention considered as a whole have not been shown to be *prima facie* obvious. Thus, this rejection of Claim 23 is traversed.

Claim 24 depends on Claim 23. Moreover, nothing fairly taught or reasonably suggested by Takeda cures the deficiencies noted above as to Yanagisawa. Therefore, the rejection of Claim 24 is traversed for the reasons noted above as to Claim 23.

With further regard to Claims 25, 26, and 28, even though these claims do not depend on Claim 23, they do include the relevant limitations of a "current sensing terminal" and an "electron injection efficiency" of a main emitter and this "current sensing terminal" as "being 0.73 or more." Thus, as Takeda cures none of the deficiencies noted above as to Yanagisawa

and to these limitations, Claims 25, 26, and 28 are also believed to patentably define over these references for the reasons noted above as to Claim 23.

In addition, Claims 27 and 29-32 recite the "current sense terminal" and other elements not fairly taught or reasonably suggested by Yanagisawa and/or Takeda considered alone or together in any proper combination. Accordingly, these claims are also believed to clearly patentably define over these references.

As it is believed that no other issues remain outstanding in this application, it is further believed that this application is, accordingly, in condition for formal allowance and an early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

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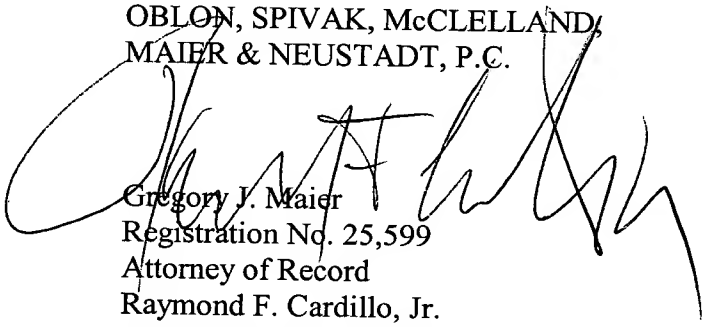

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Marked-Up Copy
Serial No: 09/684,904
Amendment Filed on:
7-19-02

IN THE CLAIMS

--23. (Amended) An injection enhanced gate transistor (IEGT) made of a semiconductor chip, comprising:

a collector formed on one side of said semiconductor chip;

a gate formed on an opposing side which opposes said one side of the semiconductor chip;

a main emitter formed on said opposing side of the semiconductor chip; and

a current sense [emitter] terminal formed on said opposing side of the semiconductor chip,

wherein electrical current from said collector is made to flow to both said main emitter and said current sense [emitter] terminal, and

electron injection efficiency at said main emitter and said current sense [emitter] terminal is 0.73 or more.

24. (Amended) The IEGT according to claim 23, wherein said gate is a trench-type gate embedded in the opposing side of said chip, and

carrier accumulation efficiency of said main emitter and said current sense [emitter] terminal in an ON state is greater than that of an insulated gate bipolar transistor (IGBT).

25. (Amended) A voltage-driven power semiconductor device, comprising:

a chip-like injection enhanced gate transistor (IEGT) having a collector on one side, and further having a main emitter, a current sense [emitter] terminal, and a gate on an opposing side which opposes said one side, electrical current from said collector being made to flow to both said main emitter and said current sense [emitter] terminal, and electron injection efficiency at said main emitter and said current sense [emitter] terminal being 0.73 or more;

a plate-like collector electrode terminal arranged on said one side of said IEGT and electrically connected to said collector; and

a plate-like emitter electrode terminal arranged on said opposing side of said IEGT and electrically connected to said main emitter,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

26. (Amended) The [IEGT] voltage-driven power semiconductor device according to claim 25, wherein said gate is a trench-type gate embedded in said opposing side of said chip, and

carrier accumulation efficiency of said main emitter and said current sense [emitter] terminal in an ON state is greater than that of an insulated gate bipolar transistor (IGBT).

27. (Amended) A voltage-driven power semiconductor device, comprising:

a chip-like voltage-driven power semiconductor element having a collector on one side, a main emitter, a current sense [emitter] terminal, and a gate on an opposing side which opposes said one side, electrical current from said collector being made to flow to both said main emitter and said current sense [emitter] terminal[, and said gate being a trench-type gate embedded in said opposing side];

a plate-like collector electrode terminal arranged on said one side of said power semiconductor device and electrically connected to said collector; and

a plate-like emitter electrode terminal arranged on said opposing side of said power semiconductor device and electrically connected to said main emitter,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

28. (Amended) The voltage-driven power semiconductor device according to claim 27, wherein said power semiconductor element is an injection enhanced gate transistor (IEGT),

carrier accumulation efficiency of said main emitter and said current sense [emitter] terminal in an ON state is greater than that of an insulated gate bipolar transistor (IGBT), and

electron injection efficiency at said main emitter and said current sense [emitter] terminal is 0.73 or more.

29. (Amended) A voltage-driven power semiconductor device, comprising:

a plurality of voltage-driven power semiconductor elements connected in series and in parallel, said power semiconductor elements including semiconductor chips and said semiconductor chips having collectors on one side, and main emitters, at least one current sense [emitters] terminal, and gates on an opposing side which opposes said one side, electrical current from said collectors being made to flow to both said main emitters and said at least one current sense [emitters] terminal;

a plate-like collector electrode terminal arranged on said one side of said plurality of power semiconductor elements, and electrically connected to said collectors; and

a plate-like emitter electrode terminal arranged on said opposing side of said plurality of power semiconductor elements and electrically connected to said main emitters,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collectors of said power semiconductor elements are pressed by said plate-like collector electrode terminal so that said collectors and said collector electrode terminal are electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter electrode terminal so that said main emitters and said emitter electrode terminal are electrically connected together.--

Claims 31 and 32 (New).